

# A FAST AND ACCURATE AUTOMATIC GAIN CONTROL FOR A WIRELESS LOCAL AREA NETWORK RECEIVER

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## Abstract

In this paper we analyze the automatic gain control (AGC) of an IEEE standard 802.11a compliant wireless local area network (WLAN) receiver. We show an efficient method to solve the problem of obtaining accurate and fast power estimates of the input signal for a huge dynamic range. In particular, we use a mixed signal approach, which has the further advantage of low power consumption. With these estimates we adjust the gains of the amplifiers to obtain the best possible signal at the analog-to-digital converters (ADCs) in the WLAN receiver. We discuss the functionality of the AGC and analyze the implemented analog and digital power estimators. For the introduced components, we provide bit- and cycle-true simulation results.

## 1. Introduction

For mobile systems such as mobile computers or personal digital assistants (PDAs) wireless communication facilities have become essential. One way to provide such facilities are wireless local area networks (WLANs), which are specified for example in the IEEE standard 802.11a [1]. In order to fulfill the requirements imposed by the regulatory bodies, we have to overcome many technical pitfalls. Particularly on the WLAN-receiver side we have to deal with power consumption constraints (battery supplied devices) and very short training sequences (frequency and timing synchronisation) which make the implementation of a fast and accurate AGC difficult. In the following we will consider a WLAN-receiver in a low intermediate frequency (Low-IF) architecture with a novel mixed-signal AGC that solves those problems.

## 2. Automatic Gain Control of a Wireless Local Area Network Receiver

In a WLAN-receiver, an AGC is used to achieve the best possible signal power at the analog-to-digital converters (ADCs) in order to minimize signal processing errors. Therefore, depending on the input signal power at the antenna of the WLAN-receiver, the low noise amplifier (LNA) and the programmable gain amplifiers (PGAs) are adjusted accordingly. Since we are not able to measure the power at the antenna on the radio frequency (RF) side, we have to estimate the power from the demodulated passband signal in an intermediate frequency (IF) stage. Three requirements on a WLAN receiver make this estimation difficult. First, we have to deal with a huge dynamic range (about 80dB) of the RF input signal. Second, we need very accurate power estimates to adjust the parameters at the LNA and the PGAs correctly in order to receive the desired signal power at the ADCs. Third, we have to find the AGC setting within a few microseconds to provide the digital part of the WLAN-receiver with a sufficiently long and stable preamble sequence for further frequency and timing synchronization processing.

In the following we present the Low-IF architecture of the WLAN-receiver and analyze the three major parts of the AGC, i.e., the controlling, the analog power estimator, and the digital power estimator.

### 2.1 System Architecture and Digital Controlling

Figure 1 shows the simplified block diagram of a WLAN-receiver in a Low-IF architecture and Fig. 2 depicts the corresponding timing diagram. All activities shown in Fig. 2 are controlled with the help of the output signals of the digital power estimator

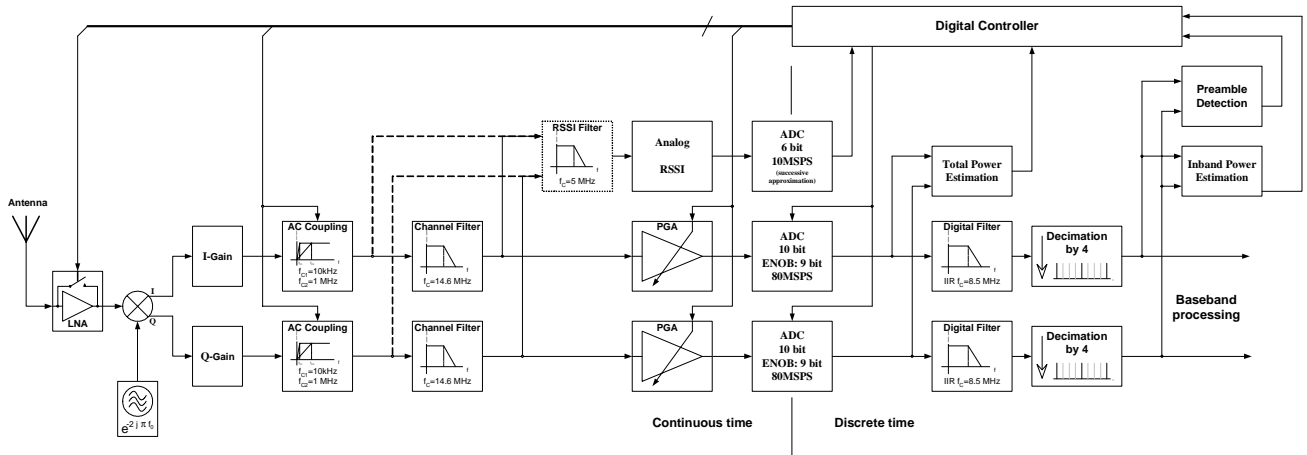


Figure 1: Illustration of a wireless local area network (WLAN) receiver implemented in a low intermediate frequency (IF) architecture with emphasis on the automatic gain control (AGC).

(total power estimation in Fig. 1), the analog RSSI and the preamble detector in Fig. 1. From Fig. 1 we can see that we have implemented an analog and a digital input signal power estimator. We have a received signal strength indicator (RSSI) followed by a 6bit ADC and 10bit ADCs followed by a digital power estimator (total power estimation block in Fig. 1). The RSSI is used to meet the dynamic and power saving requirements and the digital power estimator is used to meet the accuracy requirements within a short period of time. In the stand-by mode all unnecessary components, i.e., the 10bit ADCs and all subsequent components and most parts of the digital controller, are switched off to reduce the power consumption of the receiver. Afterwards the LNA as well as the PGAs are set to their maximum gain to achieve the maximum signal power at the 10bit ADCs even for the minimum input power of  $P_{th\_on}$  at the antenna. As soon as the input signal power at the antenna exceeds the threshold of  $P_{th\_on}$ , (cf. Fig. 2) the deactivated components of the receiver, e.g., 10bit ADCs, preamble detection and the main parts of the digital controller, are switched on. In order to detect the threshold power we use the permanently active RSSI and the low-cost 6bit ADC.

After we have detected an input signal power above the threshold at time  $t_0$ , we digitally estimate the average input power. Because of the group delay of the receiver we start the first digital estimation after  $t_0 + \tau_{ges}$  seconds over  $N$  samples to obtain the first power estimate  $P_{Est}$  (cf. Fig. 2). The analog RSSI estimates the average power simultaneously. After  $t_0 + 1\mu s$  the currently estimated average power from the RSSI and the preceding estimated average power are compared (cf. Fig. 2). If the absolute difference of both power estimates is above a certain threshold  $k$ , we take the current estimate from the RSSI. This is because for such a case we can assume that the 10bit ADCs are overdriven and the digital estimates are not correct. If the absolute difference of both power estimates is below a certain programmable threshold  $k$ , we use the much more accurate digital estimate  $P_{Est1}$ , since it is very likely that the 10bit ADCs are either only slightly overdriven or not overdriven at all.

This process is repeated every  $1\mu s$  (estimation time is chosen as a tradeoff between estimation accuracy and final AGC settling time) as long as the input signal power is above the programmable threshold  $P_{th\_on}$ , the AGC is not in steady state, and the preamble detection has not found a valid signature. The AGC

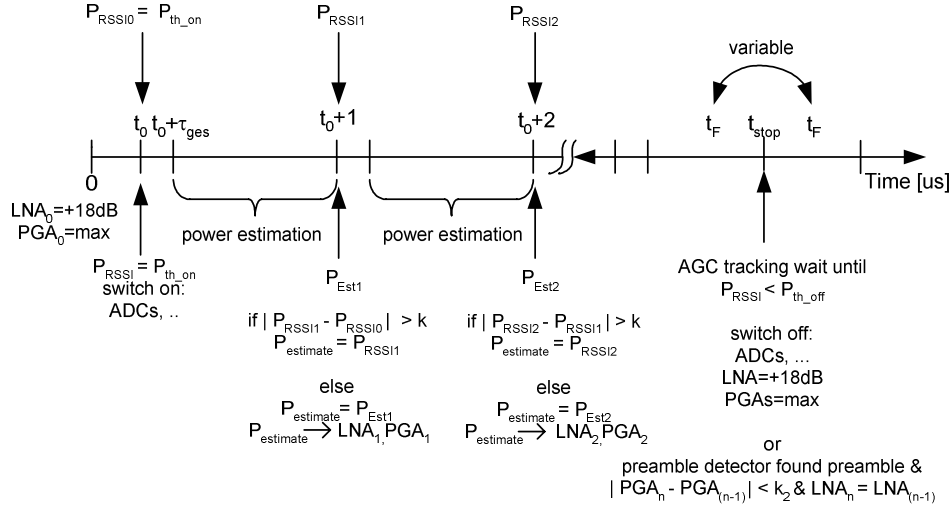


Figure 2: Timing diagram of the automatic gain control (AGC). The controlling is implemented within the digital controller block in Fig. 1.

reaches its steady state ( $t_F$  in Fig. 2) as soon as the absolute difference between the current and the preceding PGA settings falls below a certain threshold  $k_2$  and the LNA gain setting is the same as in the previous cycle ( $LNA_n = LNA_{(n-1)}$ ). After the AGC is in steady state and we have found a valid preamble, we freeze the LNA and the PGA configuration and keep it until the data burst ends.

If the input signal power is above the threshold of  $P_{th\_on}$ , we start the tracking process of the AGC again. If not we switch off the digital part. Hence, when we have strong interfering signals (blockers, strong neighbor channels) we keep tracking all the time.

## 2.2 Analog Power Estimation (Received Signal Strength Indicator)

If the antenna input signal is below a certain threshold  $P_{th\_on}$ , the 10bit ADCs and most of the digital parts are switched off to save power, which is important for battery supplied devices like mobile computers. To turn on and off those parts we utilize a simple analog logarithmic amplifier with a low cost 6bit ADC which permanently estimates the antenna input power. The estimates are used for the AGC as

well. In combination with digital algorithms, the logarithmic amplifier provides the required short settling time of a few microseconds for the optimum gain settings of the LNA and PGAs, which are shown in Fig 1. The traditional power estimation scheme is depicted in Fig. 3, where two major problems arise from an implementation point of view. The first is the high complexity of the four-quadrant multiplier (squarer in Fig. 3) and the second is the implementation of a high dynamic logarithmic compression. In [2] we have shown that for known statistics of the input signal the implementation of the analog logarithmic amplifier in Fig. 3 can be dramatically reduced if we replace the

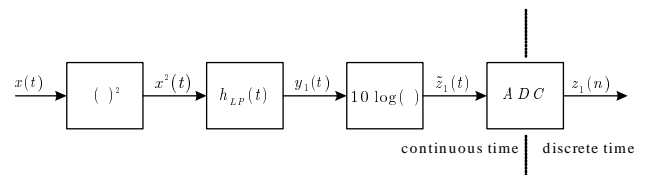


Figure 3: Traditional logarithmic power estimation. The input signal  $x(t)$  is squared, low-pass filtered, and logarithmically compressed before it is sampled by a low-cost ADC.

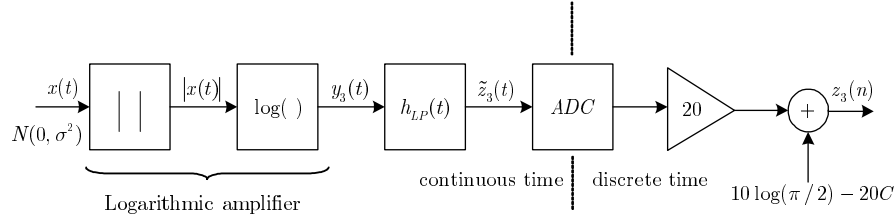


Figure 4: Power estimator with logarithmic amplifier. The order of the low-pass filter and the logarithmic block has changed, since we can implement the combination of a magnitude block and a logarithmic block very efficiently by using a logarithmic amplifier [3].

squaring block by a magnitude operator and replace the order of the low-pass filter and the logarithm block. By adding some digital post-processing the new complexity reduced analog power estimator depicted in Fig. 4 is equivalent to the conventional power estimator in Fig. 3 regarding the desired mean power [2].

### 2.3 Digital Power Estimation

We also employ a power estimator in the digital-domain, which is directly located behind the 10bit ADCs (total power estimation block in Fig. 1). This block estimates the entire power (inband-signal and all kinds of disturbers like adjacent-, non-adjacent channels and blockers) which is passed by the analog channel-filters. With the verified assumption of an independent Gaussian distributed random process  $x(n) \sim N(0, \sigma^2)$ ,  $n = 0, 1, \dots, N-1$ , we are able to calculate the logarithmic likelihood function of the  $N$ -dimensional probability density function  $p(\mathbf{x}) = p(x(0), x(1), \dots, x(N-1))$  given by

$$\ln p(\mathbf{x}) = -\ln(2\pi\sigma^2)^{\frac{N}{2}} - \frac{1}{2\sigma^2} \sum_{n=0}^{N-1} x^2(n). \quad (1)$$

From (1) we can calculate the optimal (minimum variance) unbiased power estimator [4]

$$g(\underline{x}) = \hat{\sigma}^2 = \frac{1}{N} \sum_{n=0}^{N-1} x^2(n), \quad (2)$$

where  $x^2(n)$  denotes the time dependent power and  $N$  denotes the number of samples used for the esti-

mation process. Because the estimated power in (2) is a random process itself, the minimum variance can be expressed with the Cramer-Rao bound [4] by

$$\text{Var}(\hat{\sigma}^2) = \frac{2\sigma^4}{N}. \quad (3)$$

From (3) we recognize that the power estimation is more accurate if the number of samples  $N$  is large. A serious drawback of a large number of samples  $N$  is the estimation delay which is crucial in a burst-based AGC. With the estimated power  $\hat{\sigma}^2$ , the known amplifier settings for the LNA, and the PGAs (cf. Fig. 1), we are able to precisely estimate the channel power regarding the antenna input. Thereby, we are able to control the gain in an iterative way, where we end up within an estimation error of  $|\hat{\sigma}^2 - \sigma^2| \leq 3dB$  with a probability of about 99.5%, when the AGC is in steady state. This can be seen by considering the integral over the probability density function from the lower to the upper limit in Fig. 6. The required minimum number of samples  $N$  for the power estimation process in (2) can be obtained by calculating the difference of the real power in dB and three times the logarithmic standard deviation of (3) by

$$\left| 10 \log \sigma^2 - 10 \log \left[ \sigma^2 \left( 1 - 3\sqrt{\frac{2}{N}} \right) \right] \right| \simeq 3dB. \quad (4)$$

Figure 6 depicts the power estimation samples  $\hat{\sigma}^2$  in (2) with  $N = 64$  for  $10^5$  different realizations of  $\mathbf{x}$ . The Chi<sup>2</sup>-distribution in Fig. 6 can also be ob-

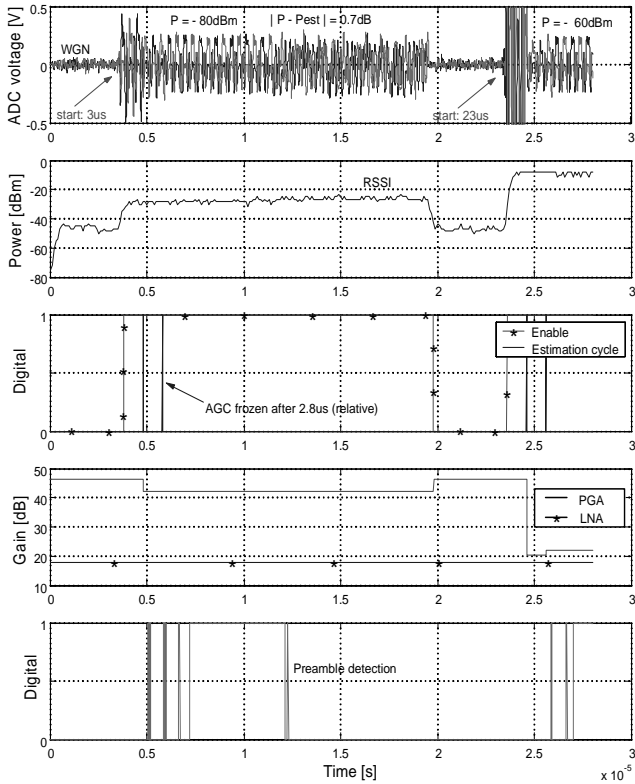


Figure 5: Simulation results for the WLAN-receiver illustrated in Fig. 1 with an additive white Gaussian noise channel (AWGN).

tained analytically by applying the inverse Fourier transform to the characteristic function of the power estimator  $g(\mathbf{x})$  in (2) [5].

### 3. Simulation Results

Fig. 5 shows the simulation results with an additive white Gaussian noise channel (AWGN) of the bit-true implemented WLAN-receiver depicted in Fig. 1. The first plot shows the input signal composed of the IEEE 802.11a standard compliant preamble sequence and the white Gaussian noise distortion. In this simulation the signal starts after  $3\mu\text{s}$  with a mean power of  $-80\text{dBm}$  regarding to the antenna input. The increasing power is observed by using the analog power estimator (RSSI) which switch on the 10bit ADCs and the main digital parts (enable signal in the third plot of Fig. 5). During the first estimation process the gains of the PGAs are decreased. After the duration

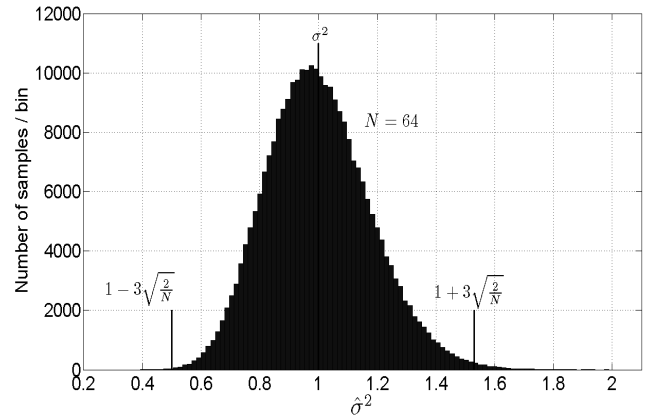


Figure 6: Normalized  $\chi^2$ -distribution for the power estimation in (2) for  $N=64$ .

of the preamble the 10bit ADCs are switched off. After a period of  $23\mu\text{s}$  a new valid burst is observed again at the antenna input. The signal power is now higher ( $-60\text{dBm}$ ) compared to the first preamble, which leads to a different PGAs setting depicted in the third plot of Fig. 5. The described AGC also works well under different environments with spectral selective disturbers like adjacent and non-adjacent channels and blockers.

### 4. References

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