A HOLISTIC DESIGN APPROACH FOR SYSTEMS ON CHIP

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ABSTRACT

We exemplify the possibilities of a holistic design approach for systems on chip. After recapitulating basic observations for next generation systems, we outline the advantages and challenges of a holistic design approach. The discussion is supported by real world examples.

I. INTRODUCTION

Today's systems on chip encompass digital, analog, and radio frequency (RF) building blocks, which are connected by data converters. Although these blocks are combined on a single chip, traditionally, their functionalities have been strictly separated. The main objective of system designers is to find the right tradeoffs between cost, configurability, performance, and power consumption. New design challenges - such as ultra wide band (UWB) communications and the Long Term Evolution (LTE) standard - and the tremendous scaling of digital CMOS technologies prompt designers to break the former separated design barriers between the building blocks [1].

Designers exploit the growing gap between analog/RF circuits and digital circuits to optimize the overall performance of the system by using two basic principles:

- Move, as much as possible, functionality from the analog/RF domain to the digital domain
- Enhance/assist the analog functionality by digital signal processing

While the first principle is mostly used to increase the flexibility of systems, e.g., software defined radio (SDR), the second is necessary to overcome performance limitations, e.g., efficiency in power amplifiers. To successfully apply these principles, the typically divide-and-conquer thinking has to be reconsidered and replaced by a holistic design approach, which is illustrated in Fig. 1 [1,2]. This approach uses cooperating blocks that support each other and exploit system knowledge [1]. For example, an ADC in a SOC system for a particular application can exploit the knowledge of the input signal statistics, the environment characteristics, and system information to compensate for impairments of the ADC. The holistic design approach allows for outperforming traditional designs, but also causes new design challenges:

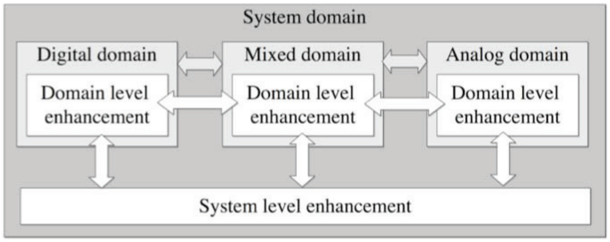

Figure 1: Holistic design approach for SOCs [1].

- The reusability of functional blocks is more difficult, as the components become more application dependent
- The design complexity increases, since engineers need knowledge from former separated fields (analog, digital, RF design)
- The simulation times increase, because the blocks are mutually dependent
- The increased complexity requires a reconsideration of the test concepts

II. EXAMPLES OF HOLISTIC DESIGN APPROACHES

In the following we discuss several examples, of holistic design approaches for SOCs. We investigate novel converter topologies, discuss new approaches for frequency synthesizers, and explore advanced enhancement techniques for power amplifiers in transmitters.

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A. Time-Interleaved ADCs

A time-interleaved ADC (TI-ADC) is a primary example for using a holistic design approach to break the performance barriers [1]. Data converters are a central part of SOC systems and often determine the performance limits in terms of resolution and bandwidth. TI-ADCs can help to overcome these performance limits, but their special structure makes it inevitable to use digital post-correction techniques [3].

The principle structure of a TI-ADC is shown in Fig. 2. It consists of M parallel channels that take samples in a time-interleaved way. Hence, periodically, for each time instant a different channel samples the value of the input signal. Therefore the requirements on each channel ADC are reduced and leading to lower power TI-ADCs with high bandwidth [4]. Unfortunately, mismatches among the channels introduce additional modulation products that significantly degrade the performance in terms of the signal-to-noise ratio (SNR) or the spurious free dynamic rang (SFDR). These modulation products are generated by the periodic change of the channel characteristics due to time interleaving [5]. However, using a holistic design approach and combining analog design and digital post-processing can circumvent these drawbacks.

In Fig. 3 the layout of a 6-bit TI-ADC (presented at ISSCC 2004) is shown [4]. The TI-ADC consists of eight channels and is designed in digital 90nm CMOS technology. It achieves sampling rates up to 600MS/s by only consuming 10mW. Without digital correction the signal-to-noise and distortion ratio (SINAD) for a sinusoidal input signal with a frequency of 329Mhz is 24.6dB, but with correction of offset mismatches the SINAD increases to 31dB [4].

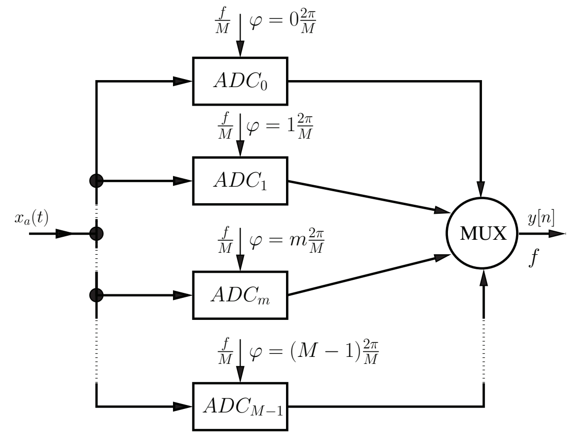

Figure 2: Principle structure of a TI-ADC.

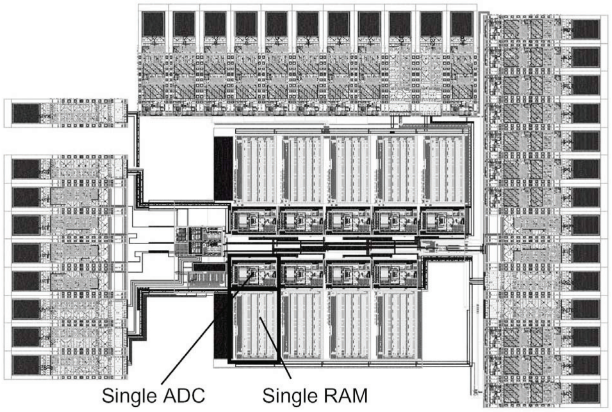

Figure 3: TI-ADC presented at ISSCC 2004 [4].

B. Pulse-width modulated ADCs

In general terms, pipeline and subranging ADCs use more silicon area than oversampled ADCs based on continuous-time sigma-delta (CTSD) and switched capacitor sigma-delta (SCSD) concepts. CTSD converters for wideband applications consist of an analog loop filter, a multi-bit flash converter, one or more DACs, and a digital decimation filter at the output [6]. The performance of such converters depends on the oversampling ratio, while the maximum available clock rate is limited by the power consumption and speed of a given technology. Integrating these converters in nanometer technologies would allow for achieving higher bandwidths without power consumption penalty; however, the integration of these converters, e.g., in 65nm CMOS, is limited by the implementation of the embedded flash converter. The main problem is the limited dynamic range of the comparators in a low voltage technology, which degrades the linearity of the quantizer [7,8,9]. Some alternative converter concepts have been explored that avoids the use of direct amplitude quantization by time encoding.

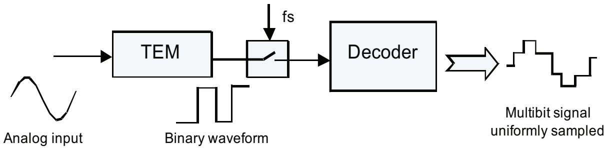

Figure 4: Analog to digital converter based on time encoding.

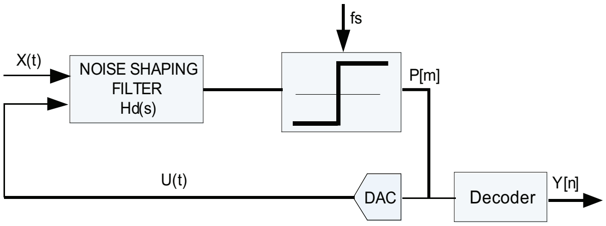

Figure 5: Block diagram of a PWM-ADC [14].

In these concepts, exemplified in Fig. 4 the amplitude information is encoded into the edges of a binary signal with a time encoding machine (TEM) [10,11,12,13]. The binary signal is then sampled to obtain a uniformly spaced sequence. To obtain the required high resolution, the sampling frequency has to be very high.

High sampling frequencies can be avoided by the pulse-width modulated ADC (PWM-ADC) shown in Fig. 5 [14], where the TEM is embedded in a noise-shaping filter of a closed loop structure, which is similar to a conventional single bit sigma-delta converter. The peak SNR in this concept is much better than in a single bit sigma-delta converter, because the quantization noise is already shaped without feedback loop.

The advantages of the architecture shown in Fig. 5 are that neither a multi-bit DAC nor a multi-bit quantizer is needed even if a multi-bit signal is generated. Another aspect is the superior dynamic range compared to a conventional multi-bit sigma delta-converter. Fig. 6 shows the chip layout for a 10-bit PWM-ADC in 65nm CMOS technology.

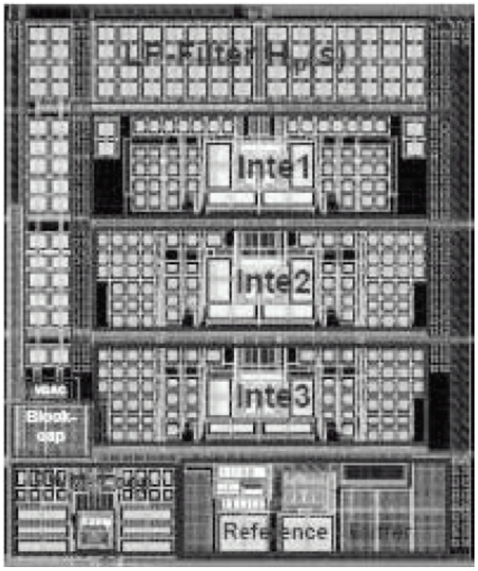

Figure 6: Chip layout of a PWM-ADC.

C. All-Digital Phase Locked Loops

The shrinking voltage headroom of CMOS technology and the demand to implement flexible transceiver architectures on a single chip, have driven the development of all-digital phase-locked loops (ADPLLs). In contrast to fractional-N PLLs, ADPLLs replace the voltage-controlled oscillator (VCO) by a digitally controlled oscillator (DCO), the analog loop filter by a digital loop filter, and the phase-frequency detector (PFD) by a time-to-digital converter (TDC). Still, ADPLLs are mixed-signal systems with analog and digital components connected by interfaces. Nevertheless, they employ the edge events of clock signals and, thus, avoid any analog tuning. In this sense, ADPLLs exploit that time resolution is expected to be superior to voltage resolution beyond 90nm CMOS technology [15]. Furthermore, the digitally intensive approach is beneficial in terms of area and power consumption, e.g., the digital loop filter requires no capacitors, in contrast to their analog counterparts. The remaining analog blocks are the DCO and the TDC, which mark the interfaces between analog and digital components. The TDC converts the time between the edge events of two clock signals into a digital quantity. Several different ADPLL architectures that utilize a TDC have been proposed, e.g. [16,17]. However, the resolution of the converters, namely the DCO and the TDC, directly affect the overall system performance. Even state-of-the-art DCO provides insufficient frequency granularity for wireless communication standards. This strong limitation can be digitally circumvented by high-rate dithering the oscillator tuning word with the aid of a digital ΣΔ modulator, which emphasizes the holistic design approach for ADPLLs.

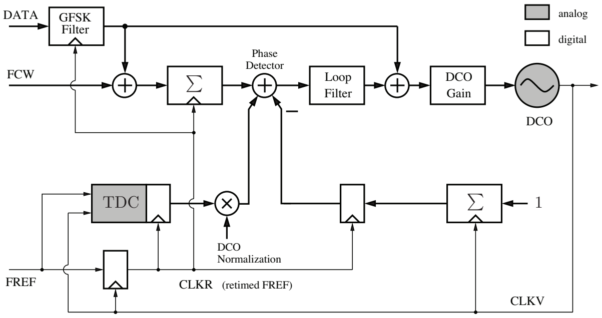

Figure 7: Architecture of a phase-domain ADPLL [17].

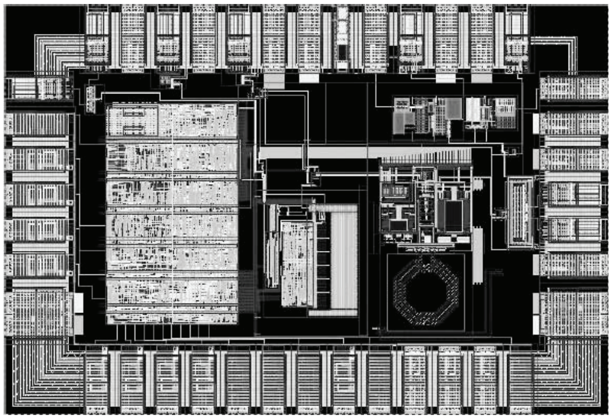

Figure 8: Chip layout of an ADPLL.

Fig. 7 shows the architecture of a phase-domain ADPLL with an LC-DCO for Bluetooth transceivers. In this architecture, the feedback path consists of a TDC, an accumulator, and a retiming mechanism, converts the analog DCO output clock signal CLKV into a digital phase signal. The digital phase detector compares the feedback phase with a digital reference phase, which is given by accumulating the frequency command word FCW. The frequency command word, i.e., the ratio between the output frequency and the reference frequency, is the input to the ADPLL and consists of 8 integer bits and 16 fractional bits. The digital loop-filter is reconfigurable in order and bandwidth and may be extended by a 4th order IIR filter. Injecting the data signal at two points, i.e., two-point modulation in the ADPLL, supports GFSK modulation according to the Bluetooth 1.0 specification.

Fig. 8 shows the chip layout of the ADPLL. The chip size is 1366µm x 926µm with a core supply of 1.2V and 10mA nominal current consumption. The phase noise is -126dBc/Hz @ 2.5MHz offset at an operational frequency of 2.4Ghz. The DCO supports a frequency range from 4.55GHz-5.27GHz with variable clock divider ratios of 2, 4, and 8. The reference frequency range is from 13MHz to 52MHz.

D. Radio Frequency Power Amplifiers

Modulation formats, which are used in modern communication standards as, e.g., in UMTS, LTE or WLAN, are usually designed for high spectral efficiency. Unfortunately, these modulation techniques generally result in highly fluctuating signal envelopes with large peak-to-average power ratios (PAPR). The large PAPR leads to an efficiency degradation of the power amplifiers (PA) and, consequently, to an efficiency degradation of the entire transmitter if one is trying to fulfill the linearity requirements. Efficiency is important for wireless handsets as well as radio base stations, because it affects production (chip area) and operating costs (power consumption) considerably. To operate the RF transmitters with an admissible efficiency (>30% linear efficiency), the final PA output stages are usually driven in their nonlinear region due to the approximate inverse relationship between the PA linearity and the PA efficiency [18,19,20]. The drawback of higher efficiency is the in-band distortion caused by the nonlinearity of the PA, which degrades the bit-error performance on

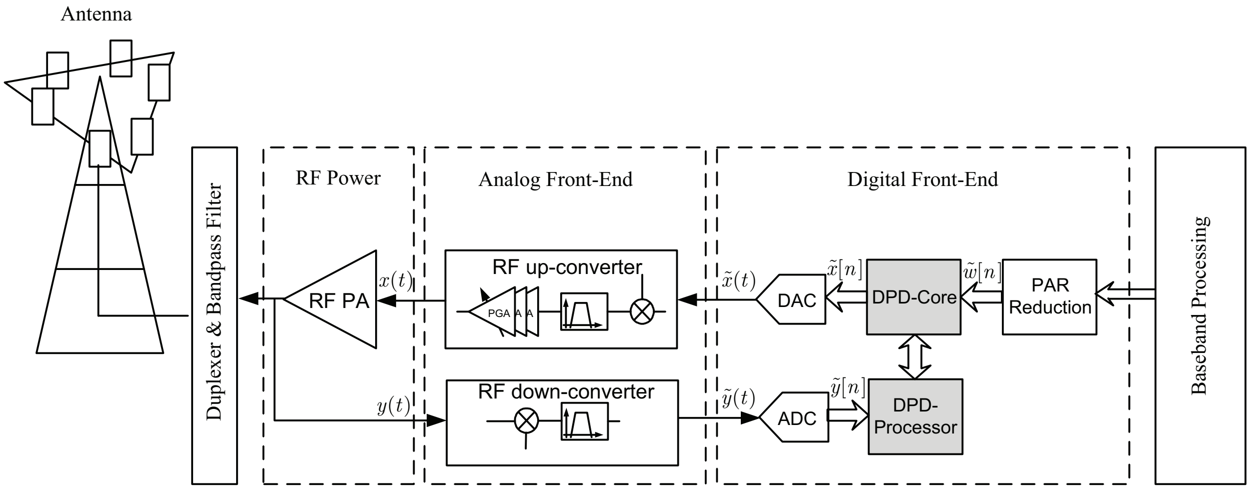

Figure 9: Block diagram of an RF transmitter for base stations [2].

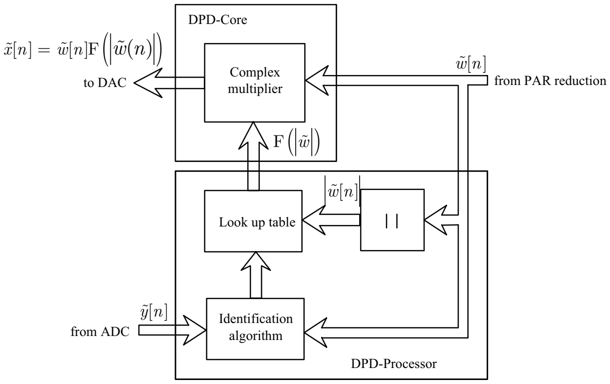

Figure 10: Concept of a digital predistorter [2].

the receiver side. Moreover, the nonlinearity causes spectral regrowth, which generally leads to unacceptable strong adjacent channel interferences. In order to comply with the spectral masks imposed by the regulatory bodies and to reduce the bit error rate on the receiver side, the RF PA must be linearized. One of the most efficient linearization techniques is digital base band predistortion [18,19,21]. A digital predistorter is a functional block in front of the PA in order to compensate the nonlinear distortion of the RF PA (DPD-core in Fig. 9). The digital predistorter incorporates the approximate inverse functional of the RF PA to obtain, in the ideal case, an overall linear system whose RF PA output signal is an amplified version of the input signal. Therefore, a PA with predistortion can be seen as a digitally enhanced DAC, where a holistic approach that encompasses knowledge of the PA and RF signal processing, the data converter and analog signal processing, and the predistorter and digital signal processing is mandatory.

If the input signal is narrowband, the predistorter can be often realized by static nonlinearities [22,23] (complex look-up table techniques as shown in Fig. 9 and Fig. 10 to obtain a sufficient performance in terms of linearity [21]. To identify the parameters within the digital predistorter (DPD-core) we need a feedback path in the RF transmitter as depicted in Fig. 9, which is composed of a cascade of a frequency down-converter and an analog to digital converter (ADC). The predistorter input signal and ADC output signals in Fig. 9 and Fig. 10 are employed to identify the parameters for the DPD core adaptively. The exact knowledge of the application and the statistics of the involved signal can significantly simplify the identification task. To further push the limits of RF PAs digital enhancement techniques are necessary. These techniques can only be successful when in a holistic design approach all components - from the digital signal to the PA output signal - are considered together. Therefore, the functional blocks become application dependent and the application moves closer to the circuits. Indeed, with an increased design complexity, we can overcome performance limits with this approach.

III. CONCLUSION

In this paper we have shown that a holistic design approach can outperform the traditional divide and conquer thinking in circuit design. It allows for new circuit architectures that benefit from digital circuit techniques. The holistic design approach can help to fulfill today's stringent system specifications, but also demands new abilities, i.e. to combine analog, digital, RF, and system knowledge, for circuit and system designers.

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REFERENCES

1. B. Murmann, C. Vogel, and H. Koeppl, “Digitally enhanced analog circuits: System aspects,” in Proceedings of the 2008 IEEE International Symposium on Circuits and Systems , ISCAS, May 2008, pp. 560–563.
2. C. Vogel, S. Mendel, P. Singerl, F. Dielacher, “Digital Signal Processing for Data Converters in Mixed-Signal Systems”, e&i Elektrotechnik und Informationstechnik, 2009, submitted
3. C. Vogel and H. Johansson, “Time-interleaved analog-to-digital converters: Status and future directions,” in Proceedings of the 2006 IEEE International Symposium on Circuits and Systems ISCAS, May 2006, pp. 3386–3389.
4. D. Draxelmayr, “A 6b 600MHz 10mW ADC array in digital 90nm CMOS,” in 2004 IEEE International Solid-State Circuits Conference, vol. 1, February 2004, pp. 45–48.
5. C. Vogel, “A Signal Processing View on Time-interleaved ADCs”, Analog Circuit Design, by Arthur H. M. Van Roermund, Herman Casier, Michiel Steyaert (eds.), Springer, in press.
6. J.A. Cherry, W.M. Snelgrove “Continuous-time delta-sigma modulators for high-speed A/D conversion: theory, practice, and fundamental performance limits,” Kluwer Academic Publishers, Massachusetts, 2000.
7. M. Steyaert, V. Peluso, J. Bastos, P. Kinget, and W. Sansen, "Custom analog low power design: The problem of low voltage and mismatch," 1997 IEEE Custom Integrated Circuits Conference, pp. 285 - 292, May 1997.

8. K. Bult, “Analog design in deep sub-micron CMOS,” Proceedings of the 26th European Solid-State Circuits Conference, September 2000.
9. C. J. B. Fayomi, M. Sawan, G. W. Roberts, “Reliable Circuit Techniques for Low-Voltage Analog Design in Deep Submicron Standard CMOS: A Tutorial”, Analog Integrated Circuits and Signal Processing, Vol. 39 (1), pp 21-38, April, 2004.
10. Roza E, “Analog to digital conversion via duty-cycle modulation”, IEEE Transactions on Circuits and Systems II, Vol. 44, no. 11, pp. 907-914, November, 1997.
11. E Roza, H Hegt, G van der Weide, A van Roermund, “An 8MHz, 72 dB SFDR Asynchronous Sigma-Delta Modulator with 1.5 mW Power Dissipation”, VLSI Circuits, 2004.
12. A. A. Lazar, L. T. Toth, “Time encoding and perfect recovery of bandlimited signals”, IEEE International Conference on Acoustics, Speech, and Signal Processing (ICASSP '03), Vol. 6, pp: VI-709-721, April 2003.
13. S. Ouzounov, E. Roza, J. A. Hegt, G. van der Weide, and A. H. M. van Roermund, "Analysis and design of high-performance asynchronous sigma-delta modulators with a binary quantizer," IEEE Journal of Solid-State Circuits, vol. 41, pp. 588 - 596, March 2006.
14. L. Hernandez, E. Prefasi, “Analog to digital conversion using a Pulse Width Modulator and an irregular sampling decoder”, Proceedings of the 13th IEEE International Conference on Electronics, Circuits and Systems, pp.716-719, December 2006.
15. L. Maurer, R. Stuhlberger, C. Wicpalek, G. Haberpeuntner, and G. Hueber, “Be fexible,” IEEE Microwave Magazine, vol. 9, no. 2, pp. 83-95, April 2008.
16. U. Vollenbruch, Y. Liu, T. Bauernfeind, T. Pittorino, V. Neubauer, T. Mayer, and L. Maurer, “Requirements for time-to-digital converters in the context of digital-PLL based frequency synthesis and GSM modulation,” in Proceedings of the Microwave Symposium, pp. 1817-1820, June 2006.
17. R. B. Staszewski, J. L. Wallberg, S. Rezeq, C.-M. Hung, O. E. Eliezer, S. K. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, “All-digital PLL and transmitter for mobile phones, IEEE J. Solid-State Circuits, vol. 40, no. 12, pp. 2469-2482, Dec. 2005.
18. P. B. Kennington, High linearity RF amplifier design. Boston, London: Artech House, 2000.
19. S. C. Cripps, RF power amplifiers for wireless communications. Boston, London: Artech House, 1999.
20. S. C. Cripps, Advanced techniques in RF power amplifier design. Boston, London: Artech House, 2002.
21. J. K. Cavers, “Amplifier linearization using a digital predistorter with fast adaption and low memory requirenments,” IEEE Trans. Veh. Technol., vol. 37, pp. 1885–1890, Dec. 1989.
22. R. Raich and G. T. Zhou, “On the modeling of memory nonlinear effects of power amplifiers for communication applications,” in Digital Signal Processing Workshop and 2nd Signal Processing Education Workshop, Oct. 2002, pp. 7–10.
23. P. Singerl and G. Kubin, “Chebyshev approximation of baseband Volterra series for wideband RF power amplifiers,” in IEEE International Symposium on Circuits and Systems, vol. 3, May 2005, pp. 2655–2658.