CLASSIFICATION BOARD FOR REAL TIME IMAGE SEGMENTATION

Johel Miteran, Remy Bailly, Patrick Gorria

Laboratory LE2I, University of Burgundy
IUT du Creusot, 12 rue de la fonderie, 71200 LE CREUSOT, FRANCE.
j.miteran@gere.u-bourgogne.fr

ABSTRACT

We present in this paper the realization of a classification board, for real-time image segmentation. The classification of each pixel is completed using a real time extraction of attributs and a geometric classification method by stress polytope training, which ensures a high decision speed (100 ns per pixels) and good performances. The decision operator has been integrated in the form of a full custom circuit, and the extraction of parameters is performed using a single high density FPGA.

1- INTRODUCTION

To increase productivity and quality on automated manufacturing lines, it is often necessary to use vision-based on-line inspection systems to automatically detect defects in the manufactured parts. In view of image segmentation in real-time (20 ms/image), we have developed a board which realises image segmentation using a FPGA and a classification circuit. The FPGA extracts significant parameters and transmits them to the classification stage.

To work at the video rate, it is necessary to take a decision in 100 ns per pixel, in accordance with the parameter-vector (figure 1).

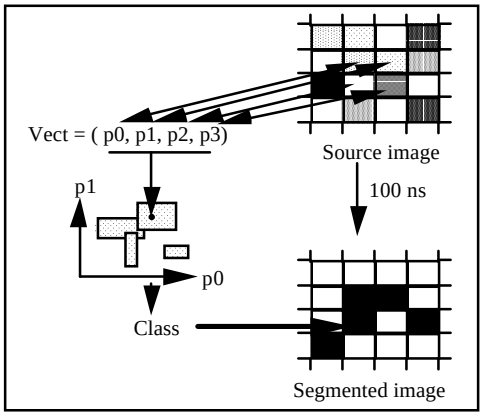

Fig 1 Low level processing

In order to improve the classification process (decision speed and stand alone operation), we have developed a parallel processor described in [7], and we present in this paper the implementation of this processor.

In the first part, we recall the classification method and the structure of the ASIC, presented in [7].

In the second part, we describe the architecture of the board which realises the real-time segmentation.

In the last part, we describe the architecture implemented in the FPGA for real-time parameter extraction, and we present some segmentation results.

2- RECALL OF THE CLASSIFICATION METHOD.

2-a- Method.

The implementation of classification by training requires two distinct steps: training and decision. We have chosen a method which divides the attribute space into a set of hyperrectangles, for which the appurtenance condition may be easily verified by simple comparators.

The attribute space is composed of the parameters defined in the next paragraph.

Sampling and determination of local stresses [6]**:** This step of the training phase consists in collecting a set $Ep=(e_1, e_2, \ldots, e_p)$ of the most representative samples from the various classes and associating a local stress $H(e_i)$ to each sample e_i, defined by an attribute vector $(x_1, x_2, \ldots, x_N)$ in an N dimensional space and its corresponding class $C(e_i)$. Figure 2 shows the samples with their n associate local stresses, after a merging phase.

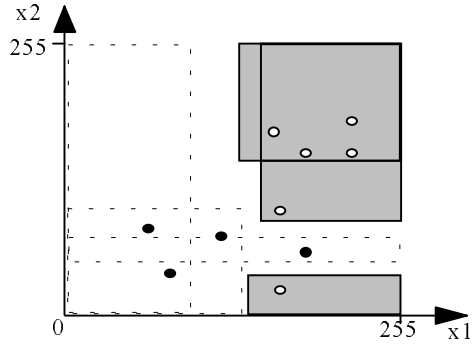

Fig 2 Hyperrectangle merging

Decision phase : The decision phase consists in allocating a class to a new attribute vector.

The appurtenance of a new parameter x_k to a given interval I_{ik} is easily verified by controlling the two following conditions : ($x_k > a_{ik}$) and ($x_k < b_{ik}$), were a_{ik} and b_{ik} are respectively the lower and upper limits of each polytope. Therefore, the verification of the appurtenance of a point P to a class Cp results in a set of comparisons done simultaneously, on each parameter, for every hyperrectangle of class Cp. The resulting logic function is:

$$C(P) = Cp \Leftrightarrow \sum_{i=1}^{i=n} \prod_{k=1}^{k=N} \left((x_k > a_{ik}).(x_k < b_{ik}) \right)$$

2-b- Architecture of the ASIC.

The architecture of the component which performs the decision operator is represented in figure 3. The ASIC contains 64 elementary cells, and each cell (fig 4) consists of an attribute vector element X_k (k=1,...,N), a lower and upper limit (a_{ik} and b_{ik} (i=1,...,64/N)) and allows verification of the appurtenance condition with respect to a given interval : $a_{ik} < X_k < b_{ik}$. If this condition is not met, the S_i output takes the logic value 0.

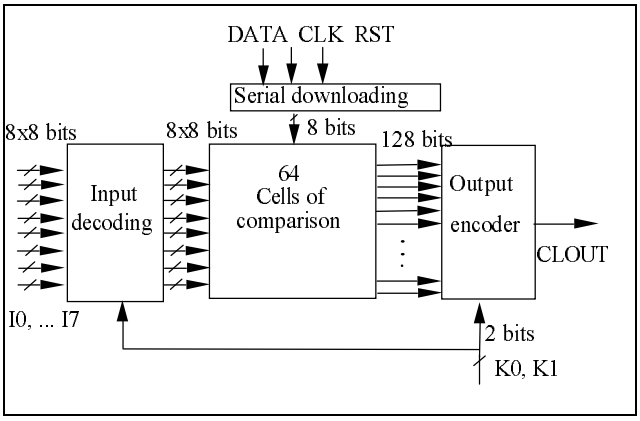

Fig 3 Architecture of the ASIC

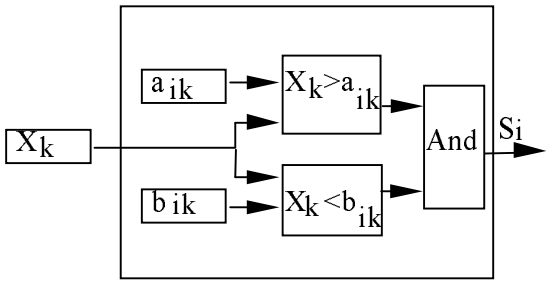

Fig 4 : Elementary Cell n°i

The a_{ik} and b_{ik} limits are downloaded in series when turning on the circuit. The signals K_1 and K_0 allow configuration of the ASIC for N=2, 4 or 8 parameters. It is possible to cascade indefinitely the components in order to increase the number of cells, and consequently an increase of the number of available polytopes.

3-ARCHITECTURE OF THE BOARD

The aim was to obtain a stand alone product: the learning phase must be realized using a PC, but the decision phase can be done without a computer.

The architecture represented in figure 2 shows the principle of the implementation of this classification ASIC.

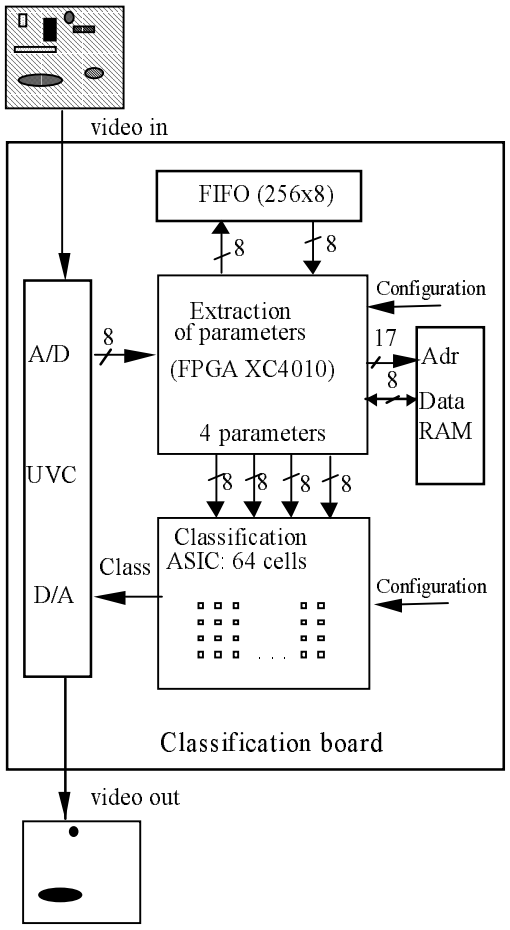

Fig 4 Principle of the implementation of the classification ASIC for image segmentation

To validate the board, we have chosen to implement two regional parameters and two local parameters. This allows to avoid a too great number of hyperrectangles (the maximum is 16 hyperrectangles with 4 paramters).

The use of the FIFO (256 bytes) allows to compute the gradient (I0) and the mean of the luminance (I1) in a local window (2x2) arround the pixel to be classified (fig. 5).

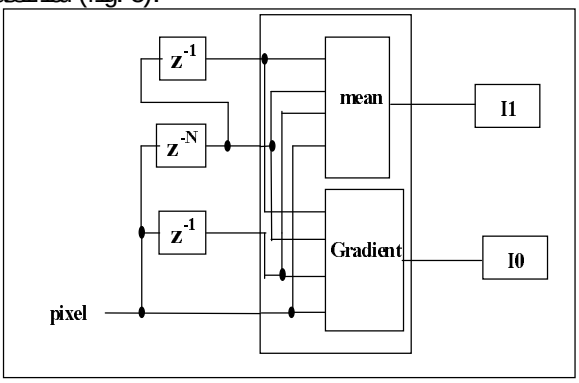

Fig 5 : Extraction of parameter sI0 and I1

The use of accumulators in the FPGA (fig 6) allows to compute the same values (I2 and I3) but in a larger window (16x16).

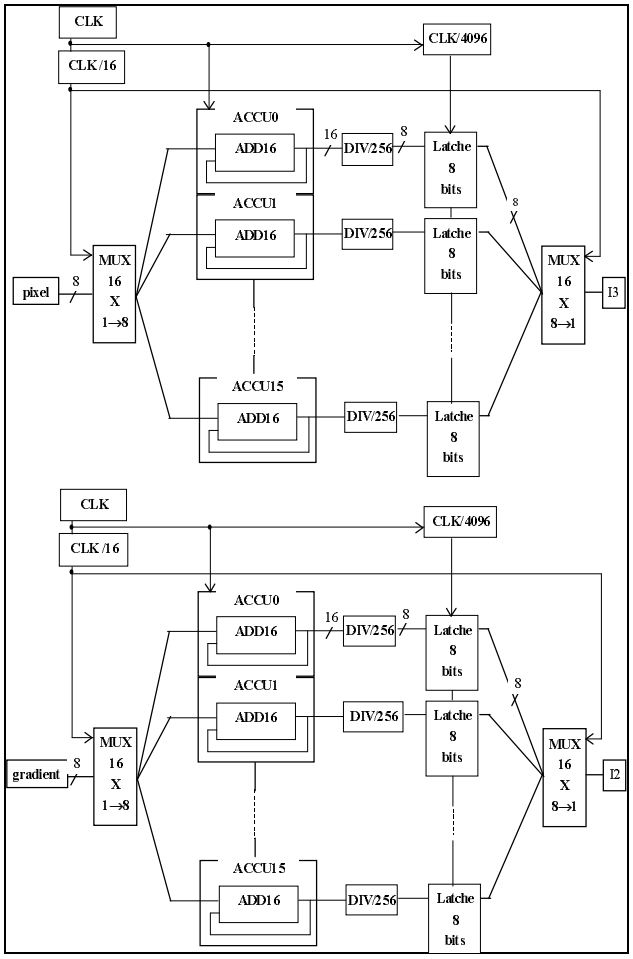

Fig. 6 Extraction of parameters I2 and I3

4- RESULTS

Figure 7(a,b,c,d) shows the effect of a real-time segmentation (texture) by self-training of stress polytopes :

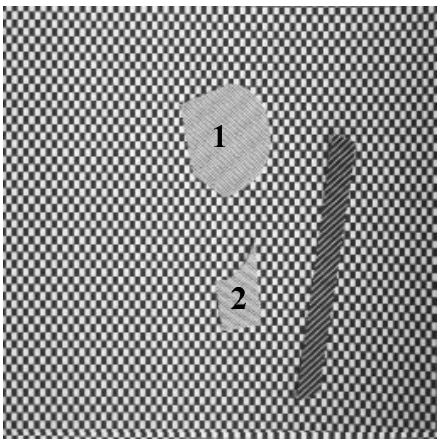

Fig 7a Training image

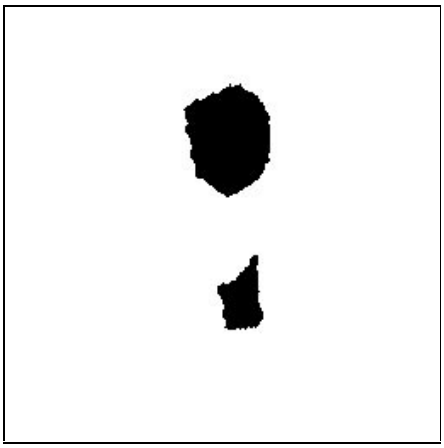

Fig 7b Segmented training image.

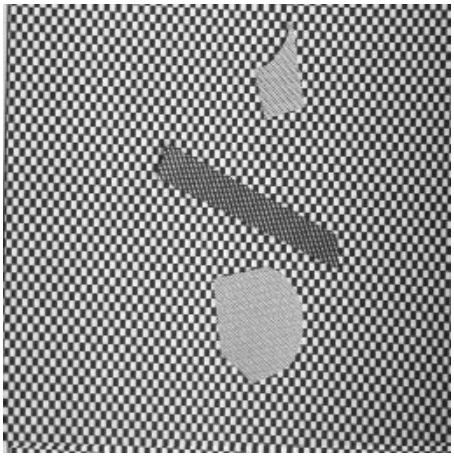

Fig 7c Example image

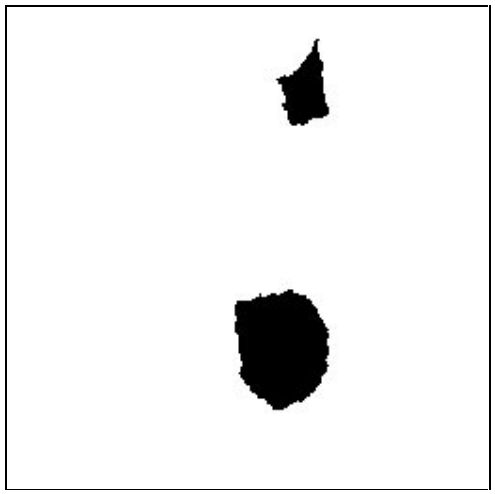

Fig 7d Segmented example image.

Figure 7a is the training image, and 7b the same image, segmented using classification. The first image was fed to the system during the training phase, with a specification of some pixels from the objects 1 and 2 for the class C0, and from the others areas for the class C1. Then we applied the decision phase on the images 7a and 7c, and we obtained the images 7b and 7d, segmented by self training of stress polytopes.

One can see that the speed of the decision in the terminal phase is independent of the complexity of the algorithm chosen in the training phase. From this information, we can choose an algorithm which gives the best performance.

5- CONCLUSION

This image processing system is mainly constituted by the CCD camera, the A/D converter, the parameter extraction ASIC (FPGA) and the classification ASIC. It is a low cost and stand alone equipment that can replace a PC computer and allows real time analysis of the defects.

The main problem for the validation of this board was to obtain a small number of hyperrectangles, because of the capacity of the ASIC (64 cells). So, we are going to design a new ASIC with 256 cells to reduce this problem and increase the performances of the system.

Finally this classification board is easy to use, fast and robust in classification, and can compete with neuronal operators, which require a very great number of components [2] [1].

REFERENCES

[1] W.E. Blanz et S.L. Gish, "A real-time segmentation system using a connectionist classifier architecture", International journal of pattern recognition and artificial intelligence, vol. 5, N°4, pp 603-617, 1991.

[2] C.E. Cox, W.E. Blanz, "GANGLION- A real Field-programmable gate array implementation of a connexionist classifier", IEEE journal of solid state circuits, vol 27, N° 3,pp 288-299, March 1992.

[3] B. Dubuisson, "Diagnostic et reconnaissance des formes", Paris, Hermes, 1990, chap 3.

[4] R.O. Duda and P.E. Hart, “Pattern classification and scene analysis”, New-York, Wiley, 1973.

[5] M. Ichino, "A nonparametric multiclass pattern classifier", IEEE transactions on systems, man, and cybernetics, vol. 9,N° 6, pp 345-352, June 1979.

[6] J. Mitéran, P. Gorria, M. Elloumi, “Architecture programmable pour l’intégration d’un classifieur géométrique”, Colloque Contrôle Qualité par Vision Artificielle, Le Creusot, May 1993.

[7] J. Mitéran, P. Gorria, M. Robert,. "Parallel processor for image segmentation", conference at MELECON 94, pp 344-346, Antalya, 12-15 April 1994.

[8] M. Robert, M; Paindavoine, P. Gorria, "An edge detection ASIC for real time defect detection.", Fifth annual IEEE ASIC conference and exhibit, Rochester, New-York, September 1992.