EFFICIENT VLSI ARCHITECTURES OF ADAPTIVE EQUALIZERS FOR QAM/VSB TRANSMISSION

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ABSTRACT

This paper proposes hardware architectures of adaptive equalizers applicable to both the quadrature amplitude modulation (QAM) and vestigial sideband modulation (VSB) systems. This paper presents digitization methods for QAM and VSB systems requiring a low hardware cost with the performance comparable to that of the algorithm employing floating-point operations. To reduce the hardware cost of the high definition television (HDTV) equalizers, we also propose a pipelined architecture that processes some parallel parts sequentially.

1. INTRODUCTION

In a digital broadcasting system, perfect reconstruction of video signals is possible as long as distortion is so small that it does not lead to incorrect decision of signals. Large distortion, however, leads to false decision, resulting in fatal effects on visibility of reconstructed video signals. An equalizer is a device that compensates for such distortion adaptively.

Quadrature amplitude modulation (QAM) and vestigial sideband modulation (VSB) were proposed for modulation methods of high definition television (HDTV) broadcasting systems [1]-[3]. HDTV equalizers require high computational complexity to implement in hardware with a large number of taps, thus we need to reduce the hardware cost by modifying equalization algorithms or hardware architectures.

The rest of the paper is structured as follows. In Section II, proposed adaptive equalization algorithms are presented. Hardware architectures are given in Section III and simulation results are shown in Section IV. Finally, conclusions are given in Section V.

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2. PROPOSED ADAPTIVE EQUALIZATION ALGORITHMS

In this section, we propose adaptive equalization algorithms driven by some modification of adaptation algorithms for simple hardware implementation, with slight performance degradation compared to the system implemented with floating-point operations.

2.1. QAM Equalization System

We decompose a constant modulus algorithm (CMA) and least mean square (LMS) algorithm for decision-directed (DD) mode and represent the weight update equations as

$$\begin{aligned} \underline{w}_r^{t+1} &= \underline{w}_r^t + 2\mu(\underline{x}_r^t e_r^t + \underline{x}_i^t e_i^t) \\ \underline{w}_i^{t+1} &= \underline{w}_i^t + 2\mu(\underline{x}_r^t e_i^t + \underline{x}_i^t e_i^t) \end{aligned} \quad (1)$$

where subscripts r and i denote real and imaginary components of a complex number, respectively, and lower-case letters represent real numbers. To use the same coefficient update module for both CMA and DD equalization modes, we adopt the 2-bit normalized values for x_r, x_i, e_r, and e_i. They are expressed with the 1-bit sign and 1-bit magnitude. They can have three integer values: -1, 0, and 1, thus the values in parentheses of (1) have five possibilities: -2, -1, 0, 1, and 2, and their non-zero minimum absolute value is equal to 1. Consequently, the corresponding increment of a filter coefficient is 2μ, thus we set μ to 2^{-B}, where filter coefficients are expressed with B bits.

We normalize x_r and x_i by means of their magnitudes $|\overline{x_r}|$ and $|\overline{x_i}|$, respectively, where the bar signifies the average value. If a received signal $\underline{X}$ follows the Gaussian distribution at each signal constellation, the mean values of magnitudes, $|\overline{x_r}|$ and $|\overline{x_i}|$, are equal to 0.5, where the upper-case letter denotes a complex number. The sign of the normalized x_r or x_i is equal to that of x_r or x_i, and the magnitude bit of the normalized x_r or x_i is set to '1' if the magnitude of a real or imaginary component of a received signal is larger than 0.5.

The 2-bit CMA error is determined as follows. First, the case is considered in which the real and imaginary components of an output Z are the same: $z_r = z_i = z$. Then the error e_{CMA} in the CMA is given by

$$e_{CMA} = z(2z^2 - R_2) \tag{2}$$

where R_2 denotes a positive real constant. Calculation of e_{CMA} needs complex hardware and computation time, resulting in much larger delay than that of a DD mode. Therefore, to reduce the computational complexity and delay, the following procedure is employed.

To obtain z for further adaptation, the increment Δw of a filter coefficient must be larger than a half of the quantization step size of a filter coefficient, i.e.,

$$\Delta w = 2\mu z(2z^2 - 0.825)(\mathrm{E}[x_r] + \mathrm{E}[x_i]) \geq 2^{-(B-1)}. \tag{3}$$

In the 16-QAM system with $\mu = 2^{-B}$ and $\mathrm{E}[x_r] = \mathrm{E}[x_i] = 2^{-1}$, equation (3) becomes

$$z(2z^2 - 0.825) \geq 1, \tag{4}$$

i.e., for real z, we have

$$z \geq 0.9637. \tag{5}$$

Therefore, we can simply threshold the equalizer output z rather than thresholding e_{CMA} in (4). Also a similar thresholding criterion can be used when z_r and z_i are not the same. Experimentally, it is observed that the performance shows little variation when the threshold between 0.92 and 0.98 is used. For simplicity, the threshold is set to 0.9375 (01111_2), i.e., the magnitude bit of the 2-bit normalized error is set to '1' when z is larger than 0.9375. A little performance degradation occurs with this proposed modification, however, it is tolerable when the decision error rate is smaller than 10% at the end of the initial equalization phase [4]. Therefore, the required performance is guaranteed if the sufficient number of bits is used.

In the DD mode, the error signal e is normalized by the maximum quantization error caused by the finite-word representation of filter coefficients. The magnitude bit of 2-bit normalized equalization error is set to '1' if the decision error is greater than the error threshold $2^{-(B-8)}$, and the sign bit is the sign of error. The width of filter coefficients for adaptation is set to 11 bits.

2.2. VSB Equalization System

Similarly to the proposed modification technique of the QAM equalization algorithm, we modify decision feedback (DF)-LMS algorithm and use the normalized quantities e, x_k, and $\hat{z_k}$ in (6) for easy and low-cost hardware implementation. The update equation are written as

$$\begin{aligned} w_k^{t+1} &= w_k^t + 2\mu e^t x_k^t, \quad -k \leq k < 0 \\ w_k^{t+1} &= w_k^t + 2\mu e^t \hat{z_k}^t, \quad 0 \leq k < L \end{aligned} \tag{6}$$

where x_k and $\hat{z_k}$ represent received and reference signals, respectively. The superscript t and subscript k signify the iteration count and filter tap index, respectively, and step size μ denotes the parameter that controls the convergence speed. For maximum performance of the proposed design, μ becomes 2^{-B} with B-bit filter coefficients. The 2-bit normalized x_k and $\hat{z_k}$ are formed with the 1-bit sign and 1-bit magnitude normalized by 0.5, which is similar to the QAM case.

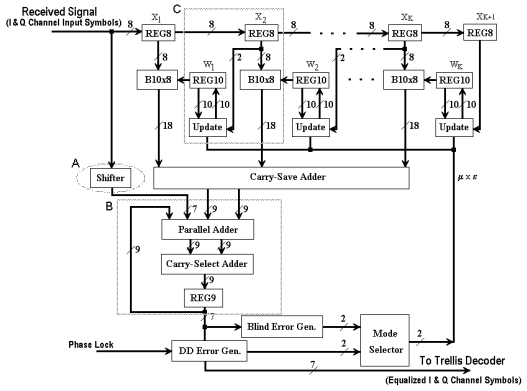
DF-LMS is basically the same as LMS, therefore, through the procedure similar to normalization of the DD mode error in a QAM equalization system, the error signal e is normalized by the maximum quantization error caused by the finite-word representation of filter coefficients. Similar to the DD mode in the QAM system, the magnitude bit of 2-bit normalized equalization error is set to '1' if the decision error is greater than the error threshold $2^{-(B-8)}$, and the sign bit is the sign of error. The width of filter coefficients is set to 12 bits for adaptation in a 8-VSB equalization system.

3. PROPOSED HARDWARE ARCHITECTURES

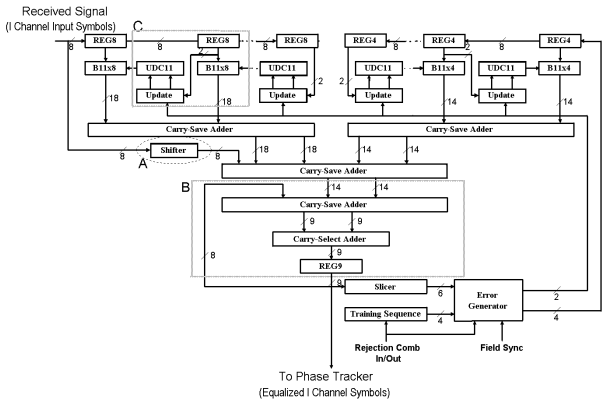
In this section, we present a basic hardware architecture that can be employed for two typical HDTV equalization systems: QAM [2] and VSB [3] equalization systems.

Two equalization systems have common basic structures such as the filter module, error calculator, equalization mode changer, and coefficient update module. Thus, the basic architecture is constructed as a framework of our design. Received signals are fed to the filter module, and multiplied by filter coefficients using the modified Booth algorithm. Carry-save adder and carry-select adder sum up the products obtained from each filter tap, then the result is fed to an error calculation module. Finally in the coefficient update module, the coefficients are adjusted by the error signal and received signals. All processes are completed in a single clock period that is the same as the sample period.

We adopt the mainframe of our design from the specific systems [2]-[3], then specify the designs through hardware mapping of equalization algorithms with previously described basic architectures. Figs. 1(a) and 1(b) show block diagrams of the designed hardware architectures of the 16-QAM and the 8-VSB equalization



(a)

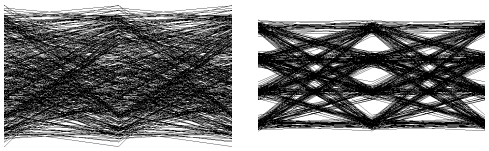


(b)

Figure 1: Block diagrams of the proposed equalizers using the pipeline concept. (a) 16-QAM equalization system. (b) 8-VSB equalization system.

systems, respectively. Fig. 1 shows the modified structures to reduce the hardware cost, where the shifter marked by A compensates for the lack of multipliers in the first filter tap, and resolutions of signals are specified for efficient hardware implementation of the modified algorithm.

Pipelining is a design technique that increases the throughput of a system by maximizing the computational efficiency with a little increase of hardware [5]-[6]. However, in our cases, the throughput is constant because of the fixed symbol rate. Hence, the hardware cost can be reduced with the same throughput by applying the pipeline concept to our design. The scheme is based on sequential summation of four Booth partial products in multipliers in four clock cycles with one Booth partial product calculator, instead of parallel processing with four products. So each symbol is calculated in every four clocks.



(a) (b)

Figure 2: Equalization results of the 16-QAM system. (a) Received signal. (b) Equalized signal.

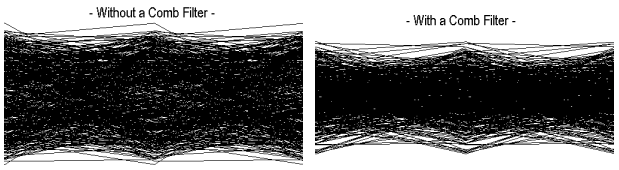
4. SIMULATION RESULTS AND DISCUSSIONS

This section shows the performance of the proposed equalization algorithms and the architecture. Our simulation is restricted to channels consisting of multi-path distortion and additive white Gaussian noise (AWG). Basically, our simulation channel is based on a 4-path model consisting of a direct path and three indirect paths. The three indirect paths are specified as follows; -12 dB attenuation with 101° phase distortion, -20 dB with $-50°$, and -25 dB with 50°. The delays of the first, second, and third paths are 0.25, 1.25, and 2.25 μsec, respectively. In addition, the channel is affected by zero-mean AWG noise with standard deviation equal to 0.02. The signal to noise ratio (SNR) of the signal transmitted through this channel is about 11 dB, which is lower than the threshold of GA-HDTV (14.9 dB) for the visibility [3].

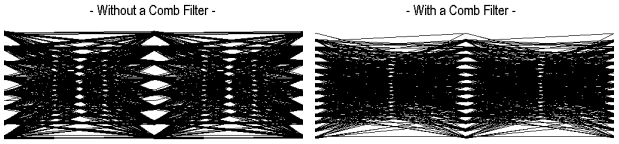
Figs. 2 and 3 are the simulation results of proposed equalizers for QAM and VSB systems. Note that the proposed equalizers give satisfactory performance although they yield a little bit degraded performance.

The designed equalizers are described using the very high speed integration circuit (VHSIC) hardware description language (VHDL) [7], structured hierarchically from behavioral or data-flow descriptions of basic functional modules, for example, register, full-adder, and so on.

Tables 1 and 2 represent the optimization results of the 16-QAM and 8-VSB equalizers, respectively, where the numbers denote the numbers of gates. These values may vary depending on applied optimization techniques and technology libraries provided by an ASIC vendor. Therefore, these numbers could be different from those of actual chips fabricated. As shown in Tables 1 and 2, our designs are optimized module by module, where '(Estimated)' represents the estimated total



(a)



(b)

Figure 3: Equalization results of the 8-VSB system. (a) Received signal. (b) Equalized signal.

number of gates of sub-modules constituting specified mother modules. Similarly, the estimated total number of gates of the entire design is listed. From Tables 1 and 2, it is noted that the hardware cost is reduced by a factor of two when the pipeline concept is applied.

5. CONCLUSIONS

The equalization systems for the HDTV receiver require massive hardware cost because of a large number of filter taps. The hardware cost is reduced by applying the pipeline concept to the equalizer architectures, i.e., by computing some parallel parts sequentially and reducing repeated hardware modules. Computer simulation results of synthesis and optimization of VHDL circuit description show that the hardware cost can be reduced by a factor of two when the pipelined architecture is applied to 16-QAM and 8-VSB equalization systems. Further research will focus on development of the real chip of the proposed architectures.

6. REFERENCES

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Table 1: Comparison of the 16-QAM Equalization System Hardware Cost

	Directly	Pipelined
1-tap Adaptive Filter Module	1328	493
Parallel Addition Modules (Estimated)	42228	42228
Error Generation Module	39	39
Partial Output Accumulator (Estimated)	·	130
Pipelining Registers (Estimated)	·	1292
Others (Estimated)	68	75
Total (Estimated)	382303	169977

Table 2: Comparison of the 8-VSB Equalization System Hardware Cost

	Directly	Pipelined
1-tap Adaptive Filter Module	740	302
Parallel Addition Modules (Estimated)	13835	8031
Error Generation Module	57	57
Partial Output Accumulator (Estimated)	·	82
Pipelining Registers (Estimated)	·	852
Others (Estimated)	135	139
Total (Estimated)	97187	45587

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