AN FPGA-BASED DATA ACQUISITION SYSTEM FOR A 95 GHZ W-BAND RADAR

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ABSTRACT

We describe a 95 GHz radar for an unmanned aerial vehicle (UAV). The radar measures vertical profiles of the reflectivity and doppler velocity of clouds, which are then telemetered to the ground for storage. Telemetry bandwidth requires that substantial real-time data processing be done on the UAV in a low-power (less than 100 watts) and small size (less than 1 cubic foot) system. A prototype was developed in less than a year, thus a flexible programmable technology was required.

Although typical remote sensing radars use DSP chips, it was determined that our power, size, performance and design-time requirements were best met using FPGA technology. Our system is based on the Giga-Ops Spectrum system which uses Xilinx FPGAs on a novel modular PCI board. Unlike numerous recent FPGA-based signal processors, this presents a new class of applications and embedded system requirements. Reconfigurable capabilities are currently being explored to support radar algorithms which can adapt to a changing environment.

1. BACKGROUND

The Microwave Remote Sensing Lab (MIRSL) at the University of Massachusetts, Amherst is currently building a 95 GHz radar that is to be operated on an unmanned aerial vehicle (UAV). This radar will measure verticle profiles of the reflectivity and Doppler velocity of clouds, and the data will be telemetered to the ground for storage. A prototype will be ready for testing in the spring of 1997. The UAV platform will be very small, placing strict requirements on the overall system. The vehicle has a limited supply of power, so the maximum allowable DC power consumption for the radar system is 100 Watts. The entire system must be contained within 1 cubic foot. Telemetry bandwidth limits the output of the DAQ to 100 Kbits/sec.

In order to meet the bandwidth limitations, a significant amount of data processing must be done in real time on the UAV. Typically, the need for real-time processing of Doppler velocity in remote sensing radars is satisfied through the use of one or more floating point DSP chips. For the UAV-mounted system, it was determined that system requirements were best met using FPGA-based technology.

2. BASIC RADAR OVERVIEW

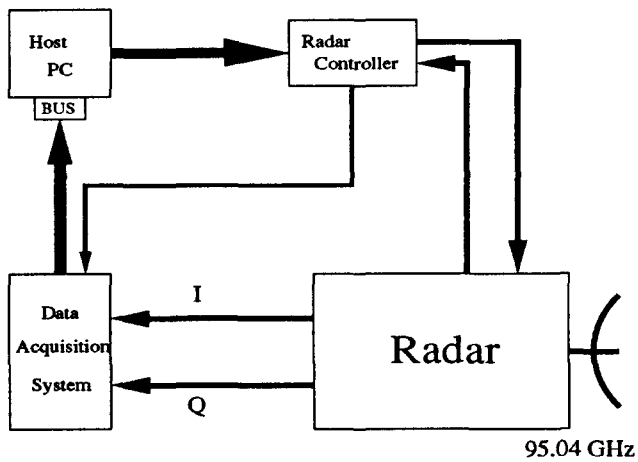

Figure 1: Radar system Block Diagram

A block diagram of the overall system can be seen in Figure 1. The radar transmits pulses of electromagnetic energy at 95 GHz. A portion of the energy is reflected and Doppler shifted by cloud particles. The reflected signal is received by the radar and downconverted to video band in phase and quadrature components (I and Q). The cloud reflectivity and frequency phase shift information are preserved through the downconversion process. This particular radar transmits at a pulse repetition frequency (PRF) of 10 to 20 KHz and a pulse length of 100 ns. The radar controller is based on programmable logic devices (PLDs)

and generates the timing signals for the data acquisition system (DAQ).

Given that the pulse length is 100 ns, it is necessary to sample I and Q at a rate of 10 MHz in order to avoid undersampling in range (distance). Each sample is called a range gate, and each pulse results in a range profile. At PRF of 20 KHz and sampling rate of 10 MSPs, there are 500 range gates per profile.

The function of the DAQ is to digitize the analog I and Q signals and compute data products related to the cloud reflectivity and Doppler velocity. Cloud reflectivity is estimated through the sum of the I and Q samples. The algorithm used to estimate the mean and variance of the Doppler velocity spectrum is known as pulse pair[1][2].

3. DATA ACQUISITION SYSTEM

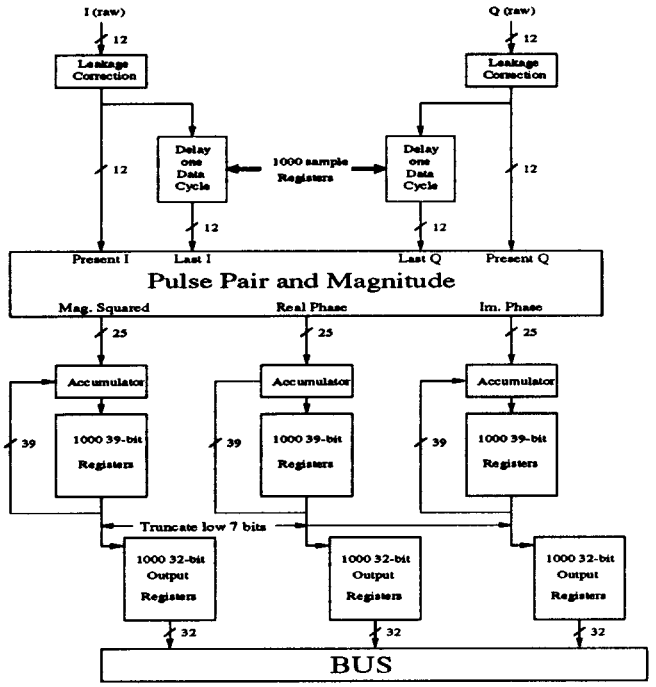

Figure 2: Overall DAQ diagram

Figure 2 shows a block diagram of the overall DAQ. At the front end of the data acquisition system is a high speed 12-bit, 40 Msample A/D converter. This chip was chosen for its speed, resolution, and power consumption. The AD4092 is currently one of the lowest power 12-bit A/Ds at this speed. The output of the A/D is sent to the FPGA-based system.

To comply with the constraints on power and size placed on the project, the Giga Ops Spectrum System [3] was investigated. The Spectrum System is a reconfigurable computing platform consisting of both hardware and software for use on a PCI-based Personal Computer. The hardware consists of a Reconfigurable Interface Card (RIC) that fits into a standard PCI slot, and small daughter-board modules called XMODS that stack on top of the RIC.

Placed on each XMOD are two Xilinx FPGAs on one side, along with four DRAMs and two SRAMs on the reverse side. Each XMOD, complete with two FPGAs and memory, is only 3.65" x 2.4". This is one of the qualities that made the Spectrum system a good platform to realize the DAQ for the UAV. When moving from the prototype to the final system to be mounted on the aircraft, a custom board will be designed that will interface between a single board PCI computer and the XMODs. The entire DAQ should take up less than 5 cubic inches. Most current reconfigurable signal processing applications are not used in embedded systems with such demanding requirements, but this system shows that FPGAs are a viable solution for small, low-power signal processing.

Within the XMODs, the data goes through the Pulse Pair and Magnitude Squared algorithm, which is described below:

Where k designates the transmit cycle (1 - 10000) and

j designates the corrected sample (0 - 499),

$$P(k,j) = I(k,j)^2 + Q(k,j)^2 \quad (1)$$

$$Re(k,j) = I(k,j)*I(k+1,j)+Q(k,j)*Q(k+1,j) \quad (2)$$

$$Im(k,j) = I(k,j)*Q(k+1,j)-I(k+1,j)*Q(k,j) \quad (3)$$

This algorithm is directly mapped to the hardware shown in Figure 3.

4. FPGA VS. DSP

A traditional data acquisition system for a remote sensing radar consists of dedicated, floating point DSP processors working alone or in parallel[4]. DSPs are instruction-set processors that are specifically engineered for signal processing algorithms. Some DSP features include separate program and data busses, one-cycle multiply-accumulate commands, and program controlled memory systems. DSPs are generally considered to be complex instruction set computers that are specialized for digital filters and transforms. DSPs come in a variety of sytles and grades, including both fixed and floating point over a wide range of speeds. For the remote sensing applications done at MIRSL, however, very fast processors are needed to handle the data rate and computations.

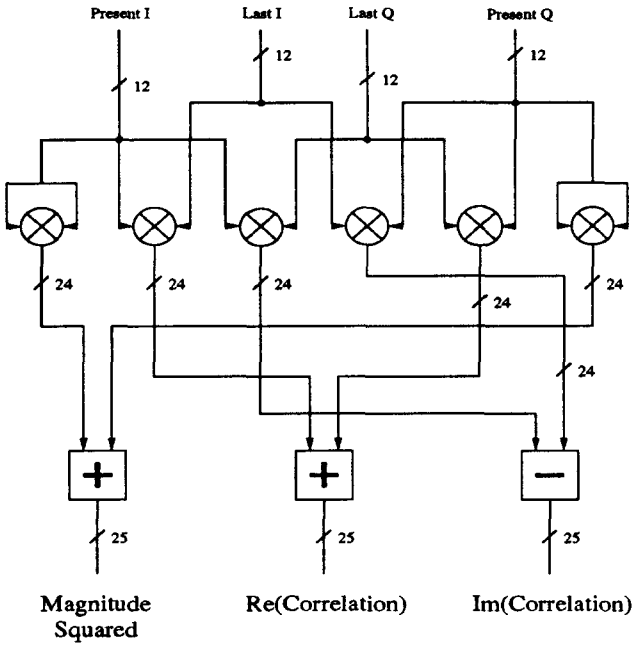

Figure 3: Pulse Pair Algorithm

One of the floating point DSP chips considered for this project was the Analog Devices SuperHarvard Architecture (SHARC) processor. It was estimated that the pulse pair algorithm, running at the desired speed, would require at least four SHARCs. Each SHARC processor is rated at 4 watts[5] running at constant speed, and thus this solution would consume 16 watts in just the DSP chips alone. Another commonly used DSP chip is the TMS320C40 from Texas Instruments [6]. As with the SHARC from Analog Devices, the pulse pair algorithm would require four C40s operating in parallel. Since the typical power consumption in a C40 is approximately 3 watts, this solution would require at least 12 Watts. In addition, C40s have a limited amount of on-chip RAM, so it would be necessary to have external memory included in the implementation, which would consume additional power.

Field Programmable Gate Arrays (FPGA) are the next generation of programmable logic devices. Presently, FPGAs are available up to 100,000 gates at speeds up to 40MHz. The traditional uses for FPGAs have been in the emulation of ASICs before they are put to silicon, and implementing any control logic between chips in a typical digital system. FPGAs have virtually replaced TTL for control and random logic, and can save designers of large ASICs the cost of verifying functionality of the chip after fabrication through rapid prototyping. Because of these attractive features, the FPGA market is probably one of the most rapidly growing areas in the semiconductor industry. Prominent FPGA vendors include Xilinx, Altera, Actel and Atmel[7].

Like DSPs, FPGAs are purchased as commodity parts and then programmed by developers for different applications. This means the design costs and risks are substantially lower than that of custom ASIC hardware. There are two types of FPGA: 1) One time programmable and 2) SRAM-programmable. The first type of FPGA uses anti-fuse technology and acts much like a large PROM. The SRAM-programmable FPGAs can be reconfigured time and time again which allows in-system changes and also the emerging technique of dynamic reconfigurability [8]. Although our current application does not exploit dynamic reconfiguration, SRAM-programmability is still a virtue for system debugging, late design specification changes, and system tuning. Possible uses of dynamic reconfiguration for the UAV project are currently being explored.

Recently, many signal processing and computational applications have been implemented using FPGAs, including a systolic FPGA-based super-computer[9] and reconfigurable general purpose computing[10]. An IEEE workshop called the Reconfigurable Architectures Workshop (RAW) is held annually to provide interaction between researchers involved with the design and applications of reconfigurable architectures[11]. Some of the reasons behind this migration towards FPGAs include the flexibility of FPGAs and the memory manufacturing process in which they are built, which is a very rapidly advancing technology.

Compared to DSPs, FPGAs require hardware design skills and hence are fairly difficult to use for the complex applications that arise in most signal processing. However, the relatively straightforward algorithms used in this application make the design problem fairly straightforward. In addition, as with DSPs, both the vendors and third party companies supply support hardware and software. The GigaOps Spectrum system attempts to make the design process using FPGAs as easy and transparent as possible. Using XLINK-OS[3], there is a specific design procedure to take a design in many forms (Schematic, VHDL, Verilog, etc.) and implement it on the Spectrum platform. Spectrum also provides a convenient interface to allow straightforward PCI communication with the FPGA co-processor from a C-program running on the host.

There are many options that FPGAs offer for future scalability and additional features in radar systems. After a working system is obtained, it may be desired to run different algorithms due to the varying environment encountered in the radar application. It has been proposed that a Fast Fourier Transform (FFT) algo-

rithm can be realized. Also, work is being done to implement floating point arithmetic in FPGAs[12]. This could be an attractive option for future use, making it possible to gain a wider dynamic range without losing the necessary precision.

5. CONCLUSIONS

Due to the constraints placed on the UAV 95 GHz radar, an FPGA based platform is being used to implement the data acquisition system, as opposed to a more traditional DSP platform. The aim behind this is to significantly reduce the power consumption, provide a very small platform that can be embedded in a one cubic foot radar system, and offer reconfigurability for future work. Secondary measurements have the FPGA system using appoximately 8 watts in the XMODS. This is still a sizable win over a typical DSP system that would most likely burn between 12 and 16 Watts in the chips alone.

FPGA-based systems for DSP have been proposed before, but most have been designed in the context of UNIX work-station accelerator boards. They have also involved fairly complex design techniques and tools. Fortunately, the improvement in FPGA semiconductor technology and the emergence of software and hardware platforms such as that provided by Giga-Ops, Virtual Computer[13] and others, means that FPGA-based DSP can be embedded in a wide range of applications.

At present, we are aware of a variety of FPGA-based DSP efforts in automatic target recognition [14], Viterbi decoding [15], image compression [14] and digital audio [7]. We are not aware of any other project to date which uses FPGA-based DSP for such demanding high-speed radar processing in such a small and low-power environment.

6. REFERENCES

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